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RM-7735-R

B. E. - IV (Sem. VIII) (E&C) Examination

May / June – 2010

VLSI Circuits

Time : 4 Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. - 4 (Sem. 8) (E&C)**

Name of the Subject :

☛ **VLSI Circuits**

☛Subject Code No. : **7 7 3 5** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the right indicate full marks.
(4) Make suitable assumption if required.

Q.1 (a) Identify following statements are True or False. Make correction if false. [05]

1. Parasitic delay is independent of gate size.
2. In 90nm process distance between source and drain is 180nm
3. Static circuits can recover easily from noise compared to dynamic circuit.
4. Hold time failure occurs in combinational circuits.
5. PMOS is constructed on p type substrate.

Q.1 (b) Answer the following questions. (One mark each) [07]

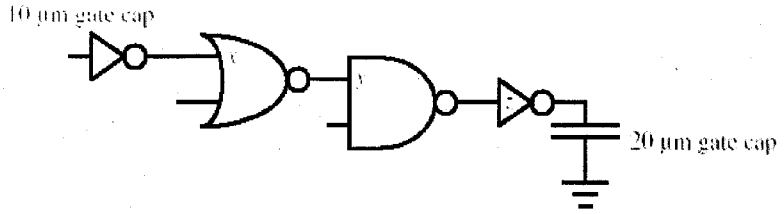
1. State effect on transistor current with increase in supply voltage of chip.
2. State effect on gate capacitance of transistor with increase in transistor width.
3. Compare power dissipation of SRAM and DRAM cell.
4. Compare drive strength of pass transistor with transmission gate.
5. Draw Lo-skew inverter.
6. Draw pseudo NMOS NOR gate.
7. Explain Die bonding.

Q.1 (c) Do as directed. (Two marks each) [08]

1. Sketch transistor level schematic for a single stage CMOS logic gate for

$$Y = \overline{(A + B)\, C}$$

2. For Circuit shown in figure (1) below, find path logical effort.



(Figure 1)

3. Explain cross talk and its implications.
4. Let resistance and capacitance of transistor are R and C respectively. If width of transistor increase by factor k identify new value of resistance and capacitance in terms of R and C.

Q.2 (a) Sketch transistor level schematic for following Boolean function, and calculate logical effort. [08]

$$Y = \overline{(A + B + C) \bullet D}$$

Q.2 (b) Discuss varios package options of IC and chip to package connection. [07]

Q.2 (a) For 3 input NAND gate discuss Elmore delay model. [07]

Q.2 (b) Compare logical effort of inverter with 2-input NAND, NOR and XOR gate. [08]

Q.3 Attempt **any three** of the following. [15]

1. Draw and explain CMOS positive level sensitive D latch.
2. Explain dynamic NOR gate with diagram.
3. Discuss carry generation and propagation mechanism.
4. Write short note on domino logic.
5. Four-input NOR gate drives 10 identical NOR gates, Calculate delay in the driving NOR gate.

Q.4 (a) Write whether statement is true or false. If false make necessary corrections. [06]

1. One entity may be assigned to many architecture bodies.
2. Structural style is closer to human thinking than behavioral style.
3. A function can have inout mode parameters.
4. If all possible values of case expression are not given as choice then the compiler produces syntax error.
5. Conditional assignment statements can not be used inside process.
6. Every if statement must have a matching end if statement.

Q.4 (b) [06]

(i) Derive subtypes from std_logic_vector to represent a nibble, byte and word.

(ii) Define two nibble objects n1,n2, one byte object B and one word object W.

(iii) Transfer 4 MSBs of W to n1

(iv) Transfer contents of n2 to the upper nibble of B in reverse order.

(v) Make bit 3 and 11 of W '1' and make others '0'.

(vi) Rotate content of of n1 right by one position using concatenation.

Q.4 (c) Answer the following in short. [08]

1. List the 9 values of std_logic.
2. If you want to use tri-state logic, which data type and package you will use?
3. State effect of input pulse having width less than inertial delay.
4. Declare 4-element array of 16-bit std_logic_vector called array_16.
5. What is transport delay?
6. State difference between procedure and function.
7. What is the difference between mealy and moore machine?
8. Explain variable in VHDL

5 (a) For VHDL code shown below, draw the block schematic of the circuit it implements. Show the circuit in terms of the known higher level blocks. (Not gate level circuit) **6**

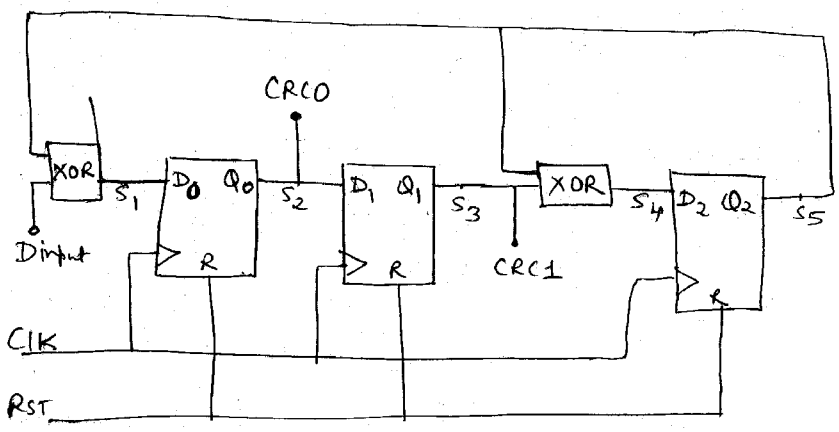
```
Library IEEE
Use IEEE std_logic_1164.all
    entity example is
    port (sel, clk, rst : in std_logic;
        I1, I2 : in std_logic,
        O3 : out std_logic);
    architecture FSM of example is
    signal x1, x2, x3 : std_logic ;
begin
    process (clk, rst, sel)
    if (rst = '1') then x2 ⇐ (others ⇒ '0')
else if    (clk 'event and clk = '1') then
        x2 ⇐ x1
        if (sel = '1') then
        x1 ⇐ I2
        else
        x1 ⇐ x3
        end if
    O3 ⇐ x2;
    x3 ⇐ x2 + I1
    end process
end FSM
```

(b) Write VHDL code to implement a 4 bit, 1 to 4 (1×4) demultiplexer with data flow model using with....select construct. **5**

(c) Describe significance of HDL in digital system design. **4**

OR

5 (a) Using behavioral description code of VHDL, implement the CRC generator circuit shown in figure. **6**



(b) For 4 bit 4 × 1 MUX. Write VHDL code using case.....when construct. **4**

(c) For VHDL code shown below draw circuit diagram. **5**

```
library ieee;
use ieee.std_logic_1164.all
entity circuit is port
cen, dir : in std_logic;
a, b : inout std_logic_vector (2 down to 0);
end circuit;
```

```
architecture con of circuit is
begin
signal temp : std_logic_vector (1 down to 0);
temp ⇐ (en, dir);
with temp select
    b ⇐ a when "11"
    ⇐ "zzz" when others
with temp select
    a ⇐ b when "10" ;
    ⇐ "zzz" when others ;
end con;
```

6 (a) Draw diagram of programmable logic array and implement following boolean function : **7**

$D_3 = \overline{A_0}$

$D_2 = A_1\overline{A_0} + \overline{A_1}\,A_0$

$D_1 = A_2\,\overline{A_1} + \overline{A_2}\,A_1$

$D_0 = A_2$

(b) Write VHDL code to implement : **8**

(i) 8 bit ripple adder (use equations)

(ii) 8 bit carry look ahead adder

OR

6	(a)	Write VHDL code to implement circuit which has two 8 bit inputs and three outputs. O_2, O_1 and O_0 . Three outputs indicate comparison between two inputs.	**8**
	(b)	With diagram explain CPLD.	**5**
	(c)	Explain VHDL test bench with appropriate example.	**5**